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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,875	06/04/2001	Christophe de Dinechin	10011596-1	5117

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EXAMINER	
VO, LILIAN	
ART UNIT	**PAPER NUMBER**
2127	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,875	DE DINECHIN ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 22 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7, 8 and 18 - 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. **Claims 7, 8, 18 and 19** recite the limitation "the inconsequential registers" in page 11, line 1 and page 13, lines 1 – 2, respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 5, 9, 11 – 16, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847, hereinafter Bugion).

7. Regarding **claims 1 and 9,** Bugion discloses a method of switching context on a processor (col. 4, lines 52 – 61), the method comprising:

saving and restoring the context under software control to memory (col. 4, lines 52 – 61: switching from and to between the HOS context and the VMM context is then carried out in the driver and in the virtual machine monitor, respectively. Col. 11, lines 30 – 52: any available memory space may be used to save context and actual storage and retrieval may be accomplished using any known technique); and

preventing the processor from changing the context while the context is being saved (col. 11, lines 30 – 52: total switch saves the state before setting it according to the target context. Col 17, lines 18 – 21: ensure that no interrupts occur during the switch).

Bugion did not clearly disclose the context is being saved and restored using an inconsequential register as temporary storage before switching. Instead, Bugion discloses that any available memory space may be used to save the information and actual storage may be accomplished using any known technique (col. 11, lines 39 – 41). It is obvious for one of an ordinary skill in the art, to relate the available memory with the inconsequential register because inconsequential register is just another type of storage (memory) that is not used by the host OS at the time of the interruption (as defined by applicants' specification page 6, lines 6 – 7). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made to modify Bugion's system to particularly use the inconsequential register instead of the available memory as disclosed in prior art as a storage.

8. Regarding **claim 2,** Bugion disclose the inconsequential register (available memory) is used as a temporary storage in lieu of a privileged register (col. 11, lines 62 – 67: context refers to state that is set and restored during the switching including the privileged registers).

9. Regarding **claim 3**, Bugion discloses the context is saved at a predetermined interruption point (col. 10, lines 31 – 48, col. 17, lines 6 – 21).

10. Regarding **claim 4,** Bugion discloses the context is switched between a host operating system and a virtual machine application (col. 4, lines 52 – 61: switching from HOS context to VMM context. Col 11, lines 30 – 52), the virtual machine application controlling the context switch (col. 11, lines 30 – 52: VMM handles directly all exceptions and interrupts that occur while executing in the VMM context. Col. 12, lines 20 – 24: the VMM completely takes over the machine and only voluntarily relinquishes control to the HOS).

11. Regarding **claim 5,** Bugion discloses the inconsequential register is used to pass information to the virtual machine application (col. 11, lines 30 – 52: total switch saves HOS context to any available memory space and changes the address space to be mapped into the VMM context. Col. 16, lines 45 - 61).

12. **Claims 11 – 16, 20 and 22** are rejected on the same ground as stated above.

13. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847, hereinafter Bugion) as applied to claims 1 and 12 above, in view of Applicants' admitted prior art.

14. Regarding **claims 6 and 17,** Bugion did not clearly disclose the context switched is using an IA-64 processor. However, Bugion discloses the process of total context switching (col. 11, lines 30 – 52) that is done in virtual machine monitor (col. 4, lines 52 – 61), in which VMM can also provide architectural compatibility between different processor architectures by using known technique (col. 2, lines 21 – 36). Furthermore, an IA-64 processor is considered a well-known architecture as disclosed in Applicants' admitted prior art (specification page 1, paragraph 4). It would have been obvious for one of an ordinary skill in the art, to implement Bugion's system with an IA-64 processor because Bugion switches total context that uses VMM which capable of providing architectural compatibility between different processor architectures (col. 2, lines 21 – 36).

15. Claims 7, 8, 10, 18, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847, hereinafter Bugion) as applied to claims 6, 9, 17 and 20 above, in view of Yamaura et al. (US. Pat. Application Publication 2001/0008563, hereinafter Yamaura).

16. Regarding **claims 7 and 8,** Bugion did not clearly disclose the temporary storage includes caller-save register or branch register. Nevertheless, Yamaura discloses a system that use link register (caller-save register) for holding an address of a source from which a subroutine call is

made and LI and LN registers (branch register, caller-save register) for holding branch destination addresses at a time of IRQ (page 6, paragraph 0110 and page 12, paragraph 209, page 5, paragraph 0082). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to particularly implement Bugion's system with Yamaura's teaching with the use of link register and/or branch register as a storage to hold the addresses of the current context information so that data can be accessed more quickly.

17. Regarding **claim 10,** Bugion did not clearly disclose the context is restored by using a branch register to perform an indirect branch. Nevertheless, Yamaura disclose a system that use a plurality of registers for storing data to undergo operation processing which can be freely written/read to/from the registers (page 5, paragraph 0082). Furthermore, Yamaura discloses that LI and LN registers (branch register, caller-save register) are used for holding branch destination addresses at a time of IRQ (page 6, paragraph 0110 and page 12, paragraph 209, page 5, paragraph 0082). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to particularly implement Bugion's system with Yamaura's teaching with the use of branch register as a storage to hold the destination addresses at a time of IRQ when restoring the context so that processing can be resumed from last interrupt efficiently and quickly.

18. **Claims 18, 19 and 21** are rejected on the same ground as stated above.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 703-305-7864. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 703-305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2127

lv
August 5, 2004

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SUPERVISORY PATENT EXAMINER
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